ABSTRACT OF THE DISCLOSURE

A cache coherency protocol that includes a modified-invalid (Mi) state, which enables execution of a DMA Claim or DClaim operation to assign sole ownership of a cache line to a device that is going to overwrite the entire cache line without cache-to-cache data transfer. The protocol enables completion of speculatively-issued full cache line writes without requiring cache-to-cache transfer of data on the data bus during a preceding DMA Claim or DClaim operation. The modified-invalid (Mi) state assigns sole ownership of the cache line to an I/O device that has speculatively-issued a DMA Write or a processor that has speculatively-issued a DCBZ operation to overwrite the entire cache line, and the Mi state prevents data being sent to the cache line from another cache since the data will most probably be overwritten.